

**Ranjeet Kumar**

**Specialization:** VLSI Design Embedded System

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**Contact no. :** 8439272037      **Gender :** Male

## Career Objective

*Seeking a challenging role in RTL Design and Software for ASIC/FPGA development, leveraging expertise in Verilog, FPGA, and digital solutions.*

## Work experience

**IIT Hyderabad (september 2024 – Present.)**

**Senior Research Fellow (SRF-Biomedical Engineering)**

- Stepper Motor Control with Raspberry Pi 4: Designed a control system utilizing a Raspberry Pi 4 board to control the movements of a stepper motor in discrete counts in a specific direction.
- Motor Controller Operations: Analyzed and worked with the ZKSM-C02 motor controller to investigate several operational modes for efficient stepper motor control.
- Worked on speech signal processing to implement ML models (Random Forest, SVM, CNN) for early detection of Parkinson's disease using existing speech datasets.
- Developed a simple GUI interface for monitoring data from an ESP32 with DHT11 sensor on the Blynk IoT cloud using a mobile application.
- Developing IoT-based web server interface for remote monitoring and analysis of medical images from Raspberry Pi, targeting applications in cell and tissue diagnosis.

**Signion System Pvt. Ltd. (9-Months):**

- Work on DSP48E2 for MAC operation.
- Performed comprehensive analysis of RF packet transmission, focusing on encryption and decryption of data packets using AES IP for secure uplink-downlink communication.
- Improved RF packet data transmission by optimizing RTL code and reducing unnecessary CDC FIFO by smart FSM code design for efficient module replication.
- Designed RTL code for LED blinking/toggling sequences, with hardware implementation on FPGA Board ZCU102.
- Developed a project utilizing BRAM memory to store and manage data, interfacing it with a FIR compiler IP for executing convolution operations with a 16-tap filter coefficient.
- Eliminated redundant .coe file (coefficient file) in a Vivado generated TCL script by TCL command.
- Developed and integrated the filter block utilizing FIR IP and Delay subblocks to process input data(I,Q) generated from MATLAB code, ensuring seamless signal transformation.

**VSDsquadron Mini RISC-V Internship [VLSI System Design | May24-July 24 ]**

- Developed a counter displaying sequences from 0000 to 9999 using the VSDsquadron RISC-V development board and TM1637 display driver.
- Ensured efficient data transfer between the VSDsquadron board and the TM1637 display driver using the I2C protocol.
- Configured PD4 and PD2 GPIO pins for TM1637 and managed 5V power and ground connections.
- Leveraged the CH32V003 chip operating at 24MHz with a 32-bit RISC-V core (RV32CE), 2KB SRAM, and 16KB flash memory.
- Wrote application code to control the count sequence display and adjusted delay settings for count speed.

**Workshop: Training [NIELIT Calicut (C2S Programme under Meity) ]**

- Gained hands-on experience with the Nucleo STM32G474RE MCU.

- Mastered the configuration of GPIO pins and clock settings using the STM32Cube IDE environment.
- Developed expertise in manipulating clock frequencies using Prescaler to decrease and PLL to increase.

### Educational Qualifications

Examination	University/Institute	Year	CPI / %
M.Tech.	NIT Raipur (Chhattisgarh)	2023	8.73
B.Tech	Roorkee Institute of Technology, Roorkee (Uttarakhand)	2016	68.96%
Intermediate	Woodbine Modern School, Darbhanga (Bihar)	2011	65.60%
Matriculation	Jawahar Navodaya Vidyalaya, Madhubani (Bihar)	2009	83.60%

### Skills

Verilog	Scripting (TCL , Python)	RTL Design (IP integration)
C / Embedded C	UART / SPI/ I2C	DSP48E2 MAC Operation
AMBA Protocol (AXI / AHB /APB )	Matlab (Basic)	Xilinx IP (AES/FIR Compiler/FIFO)

### Courses & Certifications

Digital IC Design (N.P.T.E.L)	Hands-On ZYNQ: Mastering AXI4 Bus Protocol (Udemy)
Verilog HDL (N.P.T.E.L)	System on Chip Design using VIVADO : ZYBOZ-10 (Udemy)
Embedded Design (NIELIT Calicut)	VSDsquadron Mini RISC-V Internship (VSD Pvt.Ltd )

### Publications

Power Control in Device -to-Device Communications using Deep Deterministic Policy Gradient (IEEE-Conference)